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Abstract: The organic Poly (Vinylidene Chloride co-Methyl Acrylate) co-polymer was made on n-type InP substrate with gold (Au) as capping layer and thereby electronic modification at the interface structure was studied as a function of annealing temperature. It has been observed that Poly (Vinylidene Chloride co-Methyl Acrylate) co-polymer-based devices performed good rectifying behaviour and with the Poly (Vinylidene Chloride co-Methyl Acrylate) co-polymer layer increases the effective barrier height (BH) by affecting the space charge region (scr) of the device. In the present study, the electrical properties of Poly (Vinylidene Chloride co-Methyl Acrylate) co-polymer on n- type InP Schottky device are analyzed at different annealing temperatures using J-V and C-V techniques. The obtained BH is 0.75 eV using J-V, 0.87 eV using C-V and the ideality factor is 1.47 on Au/P(VDC-MA)/n-InP Schottky device. Upon, annealing the device at 100 °C for 1 min in nitrogen ambient the obtained BH is 0.79 eV using J-V and 0.90 eV using C-V and ideality factor is 1.32. Further annealing the device at 150 °C in N₂ ambient for another 1 min, the obtained BH is 0.86 eV using J-V, 0.97 eV using C-V and ideality factor is 1.12. From the above analysis, the Au/P(VDC-MA) Schottky device electrical properties are properly increased on annealing at 150 °C.

Keywords: n-type InP; Au/P(VDC-MA), Schottky device, J-V and C-V electrical characteristics.

1. INTRODUCTION

In semiconductor industry, Metal-Semiconductor (MS) rectifying contacts are most widely used. Performance of the devices by fabrication of Schottky device is utmost important. Therefore, the fabrication of high quality Schottky contacts is essential to improve the performance of the device. The performance and reliability of these devices at the interface of MS is essentially important. Ideal interface may be defined as the equilibrium process between two materials, where abrupt transition among bulk material properties of individual layer is characterized by BH. The BH is defined as difference of the majority carrier band of the semiconductor and the Fermi level at the interface [1, 2].

Most promising research achievement on polymers is the synthesis of conducting polymers. This conducting polymer has initialized the microelectronics/opto electronic and nano science applications like light emitting diode (LED), field effect transistor (FET), photo voltaic (PV) cells, lasers and electromagnetic interference shielding, etc [3-6]. Upon doping with different ions, the conducting polymers and their doped derivatives displayed high electrical conductivity. This prompted the researchers to fabricate devices with good electrical properties leading to the fabrication of polymer possessed solid state electronics. Schottky devices are based on conducting polymers like poly (pyrrole, thiophene, vinyl chloride and aniline) and are given due importance, because of improvement in BH and electrical characteristics, besides of some unfavorable poor environmental stability, brittleness, extension/elongation with less process ability [7]. Although they have favorable

electrical properties, but most of them exhibit poor environmental stability, brittleness, long elongation and poor process ability. The known fact at interface of a MS has a vital attributes on device stability, performance and reliability. An insulated oxide layer will be grown during the fabrication of a MS contact. This insulated oxide layer will transform the MS into a metal/Insulated/semiconductor device. Hence, sandwiching an organic film in between metal and inorganic semiconductor knowingly, thereby modify electrical characteristics of a device. SBH of MS contacts can be modified by net effective dipole charges at interface of organic and inorganic semiconductor. Various researchers observed that the organic films have improved the electrical properties of Schottky devices using an organic film [8-12] Several studies revealed modification and/or control of BH by inserting organic film/inorganic semiconductor as an insulating layer was obtained by chemical passivation method at the interface [13,14]. In a nutshell organic film dominates the charge barrier deposited at MS interface, by preventing direct contact of metal with semiconductor. Besides the metal/organic/inorganic semiconductor turns abruptive and uncreative [15]. The organic film on inorganic semiconductor devices may enhance the device properties at the fabrication process.

In recent years, many works to enhance the BH, by deposition of organic film on MS structure [3, 16, 18]. Angappane et al. [16] synthesizing polymethyl methacrylate (PANi-PMMA) blended with polyaniline for fabrication of Schottky barrier devices and studied junction electrical characteristics by using I-V and C-V measurements. Ashok Kumar et al. [17] investigated the deposition of Phthalocyanine (CuPc) film on Pt/n-Ge Schottky devices and studied electrical characteristics using I-V and C-V measurements and concluded the improved BH appreciably, which was significantly greater than its conventional Ge Schottky diode and revealed improved BH in the annealing temperature range of 100 $^{\circ}$ C -300 $^{\circ}$ C, upon insertion of poly vinyl alcohol between MS structure than the conventional Au/n-InP Schottky device.

2. EXPERIMENTAL PROCEDURE

In the present work, deposition of Poly (Vinylidene Chloride co-Methyl Acrylate) on upper side polished n-type InP semiconductor wafer, having a doping density of 4.5×10^{15} cm⁻³. The small pieces of wafer have been subjected to chemical RCA cleaning usually performed on the semiconductor before high temperature process steps. Here the small pieces are sequentially dipped in trichloroethylene, acetone and methanol for 5 min each in an organic solvent using ultrasonic agitator bath. After RCA clean, the small pieces are kept in running deionized (DI) water and finally each small piece is dried in N_2 flow. To remove oxides formed on the polished surface, they are dipped in HF:H₂O (1:10) solution and again kept in running DI water for 30 sec and dried again in N₂ flow. Ohmic contact was made by thermal evaporation method by low resistivity Indium (In) on the rough side of wafer. Later the small samples are subjected to Rapid Thermal Annealing (RTA) for uniform distribution of ohmic contact at 350 °C for 3 min in N₂ ambient. After the RCA cleaning steps and ohmic contact, the Poly (Vinylidene Chloride co-Methyl Acrylate) solution is synthesized by adding 250 µl of Poly (Vinylidene Chloride co-Methyl Acrylate) organic compound solution in (0.5 wt% in tetra hedrofiron (THF)) the compound solvent uniformly deposited by using the spin coater on the polished surface of wafer pieces. After spin coating, the pieces of wafer is set for drying of solvent in N_2 flow for 1 hour. The P(VDC-MA) of 250 µl was taken due to the parameters like solution concentration, ability of film forming, area, thickness of organic film P(VDC-MA) on n-InP and obtained thickness was calculated as 23.0 nm by using profilometer. A circular diameter hole metal mesh of 1 mm diameter was taken for Schottky contact of gold (Au) with a 30 nm thickness obtained by electron beam evaporation technique at about 6×10^{-6} mbar pressure. Schottky contacts separately annealed at 100 °C and 150 °C respectively under rapid thermal annealing system at a temperature of 350 °C, for about 1 min duration in N₂ ambient. The current density-voltage (J-V) and capacitance-voltage (C-V) characteristics are measured using Semiconductor measuring System.

3. RESULTS AND DISCUSSION

3.1. Current Density-Voltage (J-V) Characteristics of Au/Poly (Vinylidene Chloride co-Methyl Acrylate) /n-InP Schottky structure

Figure 1 shows the forward and reverse current density-voltage (J-V) characteristics for Au/P(VDC-MA)/n-InP Schottky devices measured at various annealing temperatures. It can be inferred that all Au/P(VDC-MA)/n-InP Schottky devices showed uniform properties under different temperatures. The J-V characteristics can be derived by applying the relation of thermionic emission for metal-semiconductor having low doping concentration and the equation is given by

$$J = J_o \exp\left(\frac{qV_d}{nkT}\right) \left[1 - \exp\left(-\frac{qV_d}{kT}\right)\right]$$
(1)

and

$$J_{0} = A^{**}T^{2} \exp\left(-\frac{q\phi_{bo}}{(kT)}\right)$$
⁽²⁾

where J_o is saturation current density, ϕ_{bo} is SBH, q is charge of electron, V_d is applied voltage, k is Boltzmann's constant, n is ideality factor, T is absolute temperature and A^{**} is the effective Richardson's constant. From theoretical considerations, A^{**} equals to 9.4 Acm⁻² K⁻² when the effective mass is m^{*}=0.078 m_o, mo is the rest mass of InP semiconductor, which is used for ϕ_{bo} [19]. Further the BH is derived from the equation

$$\phi_{bo} = \frac{kT}{q} \ln \left(\frac{A^{**}T^2}{J_o} \right)$$
(3)

If we know the effective Richardson's constant A^{**} , the value of ϕ_{bo} may be obtained from J-V curves of the figure 1.



Fig1. Plot of J-V curves of current density-voltage (J-V) characteristics of the Au/P (VDC-MA)/n-InP Schottky structure.

The obtained plot of $\ln(J)$ versus V is a straight line having a slope of q/(nkT) and intercept of J_0 on yaxis. Four orders magnitude at $\pm 1V$, of current rectification was shown by Schottky devices. Further Au/P(VDC-MA)/n-InP Schottky devices having leakage current densities of 6.950×10^{-5} , 8.605×10^{-6} and 3.171× 10⁻⁵ Am⁻², corresponding to as-deposited, annealed at 100 °C and annealed 150 °C contacts under reverse bias of 1V. When annealed at 150°C, the Au/P(VDC-MA)/n-InP Schottky device showed decrease in leakage current density, which infers that the SBH is slightly increased when compared with the as-deposited SBH (is 0.75 eV) and annealed at 100 °C SBH (is 0.79 eV). From calculations of SBH, it may be concluded that annealing at 150 °C SBH is 0.86 eV, which is optimum for Au/P(VDC-MA) Schottky device. The ideality factor 'n' is obtained by the current density and forward bias voltage, when forward current and effective series resistance is small using the relation n = (q/kT)(dV/d(lnJ)). The ideality factor of as-deposited Au/P(VDC-MA)/n-InP Schottky device is 1.47, improved to 1.12 when annealed at 150 °C, further enhanced to 1.32 while annealing at 100 °C, for about 1 min in nitrogen ambient. This shows that the devices having ideality factors greater than unity. The probable reason of greater values of ideality factor can be attributed that at interfacial layer, there is a potential drop because of excess recombination current between organic and inorganic layers [20]. The other probability of greater values of ideality factor of more than unity is due to inhomogeneities of P(VDC-MA) organic film thickness. Series resistance and charge distribution at the interface may be non-uniform there by values of ideality factor is greater than unity [21]. Generally larger ideality factor cannot be attributed to the transport phenomenon of the thermionic emission relation, but may also be due influence of secondary charge mechanism at interface. A physical barrier may be assumed to be formed at the interface of the metal and inorganic n-InP substrate, thereby not allowing the metal to be in direct contact with n-InP substrate. This P(VDC-MA) organic film deposition may be the reason for slight enhancement of BH at interface in the bilayer device. Passivation can be explained by an interface dipole, electrical characteristics of Schottky devices is influenced by the series resistance parameter at the interface, which is dominated by non-ideal forward bias current-voltage. The best known reason of a specially fabricated Schottky device is definitely contains a thin interface oxide layer, which is obtained by chemical synthesis or mixing or evaporation deposition of a metal using high vacuum deposition chambers between the metal and the semiconductor (or conducting polymer/semiconductor). Strong influence on device characteristics may be due to this interfacial layer tending to increase series resistance in given device which is observed in non-linearity regime in forward plot of J-V curves [22]. A method developed by Cheung and Cheung [23] is used to calculate series resistance R_s, with this parameter we can plot concave curvature with forward bias condition to get current density voltage plots when large voltage is due to R_s. It is well known that the downward concave curvature of the forward bias current density-voltage plots at sufficiently large voltage is caused by the presence of the effect of interface states, which are in equilibrium with the semiconductor [24]. According to Cheung method, the J-V characteristic due to thermionic emission (TE) under forward bias considerations of Schottky device, where the voltage drop across series resistance of the device, which can be expressed as

$$J = J_o \exp\left[\frac{q(V - IR_s)}{nkT}\right]$$
(4)

where the IR_s term is the voltage drop across series resistance of device. The values of the series resistance can be determined from the following equation

$$\frac{dV}{d(\ln I)} = \frac{nkT}{q} + IR_s \tag{5}$$

From eq(5), A plot of $dV/d(\ln I)$ with I should be a linear and obtained R_s as slope and nkT/q as y-axis intercept. The fractional change in various values of ideality factor 'n' obtained from the ln(I)-V and the $dV/d(\ln I)$ -I curves and are listed in Table-1.

Table1. Au/P (VDC-MA)/n-InP Schottky device with varying annealing temperatures and obtained values of leakage current density, SBHs (J-V, C-V and Norde), series resistance (from dV/d (lnI) vs I) and ideality factor (n).

Sample Temperature	Leakage	Schottky barrier heights (eV)				Carrier	Series
	current					concentration	resistance
	density at (-1V) Acm ⁻²	ф _{ьо} (J-V)	ф _{ьо} (С-V)	ф _{ьо} Norde	Ideality	N _d cm ⁻³	dV/d(lnI)
					factor		vs I
					n		R _s
as-dep	6.950× 10 ⁻⁵	0.75	0.87	0.81	1.47	8.509×10 ¹⁵	174
100 °C	8.605×10 ⁻⁶	0.79	0.90	0.91	1.12	3.543×10 ¹⁵	68
150 °C	3.171×10 ⁻⁵	0.86	0.97	0.95	1.32	5.409×10 ¹⁵	111

This characteristic may be attributed due to the presence of R_s i.e voltage drop across interface oxide layer.

Using the conventional analysis like Norde where higher values of series resistance prevents correct calculation of BH from standard ln (I)-V plot. Using Norde analysis, F (V) with V is plotted in figure 2 using the equation

$$F(V) = \frac{V}{2} - \frac{kT}{q} \ln \left[\frac{I(V)}{AA^{**}T^2} \right]$$
(6)

The effective SBH is given by

$$\phi_{bo} = F(V_{\min}) + \frac{V_{\min}}{2} - \frac{kT}{q}$$
⁽⁷⁾

Where F (V_{min}) is the minimum value of F(V) and V_{min} is the corresponding voltage. From the Table-1 it can be inferred that the values obtained are in good agreement with those obtained by the J-V characteristics.



Fig2. Plot of F (V) versus V for Au/P (VDC-MA)/n-InP Schottky contacts annealed at different temperatures.

3.2 Capacitance-voltage characteristics and the effect of Au/P(VDC-MA)/n-InP Schottky device

To know how rectifying contacts behaves at interfaces, we need non-destructive technique like capacitance-voltage electrical characterization. In this technique the space-charge region has less capacitance in forward bias condition, which is assumed a fundamental fact. The excess capacitance is difference of calculated and space charge region in forward bias, which is caused at interface layer, may be attributed due to the formation of crystal lattice faults (dangling bonds) in diffusion of atoms and lattice faults at MS interface. In this work, capacitance-voltage (C-V) technique is applied at a frequency of 1 M Hz and at room temperature for as-deposited and for annealed samples of Au/P(VDC-MA)/n-InP Schottky device. A depletion layer is assumed to be formed at the MS interface, which is presumed as bias-dependent capacitance. In Figure 3, which is a plot of $1/C^2$ versus bias voltage of as-deposited and contact annealed at two different temperatures. The tangent to the $1/C^2$ versus V plot emerged essentially from a point in the voltage axis. The $1/C^2$ versus V plot, showed that with increasing applied bias, the capacitance C decreases slowly, because deep-level traps are increasingly exposed due to reverse bias in the depletion region. The C-V characteristic equation for Schottky device is given by [25]

$$\frac{1}{C^2} = \frac{2(V_d + V_r + kT/q)}{q\varepsilon_s A^2 V_A}$$
(8)

where V_{bi} is built-in voltage, A is area of the Schottky contact and ε_s is permittivity of the semiconductor ($\varepsilon_s = 11\varepsilon_o$). The x-intercept of $(1/C^2)$ versus V plot yields V_o and V_o is related to the built in potential, $V_{bi} = V_0 + kT/q$, k is Boltzmann constant, q is charge of electron, T is absolute temperature, V_d is the potential difference between the Fermi level and top of the valance band in the neutral region of n-InP.



Fig3. Plot of $1/C^2$ versus V for the Au/P (VDC-MA)/n-InP Schottky contacts annealed at different temperatures.

The barrier height ϕ_{CV} is given by

$$\phi_{CV} = V_{bi} + V_d$$

Where the density of states in the conduction band edge is given by $N_c = 2(2\pi m^* kT / h^2)^{3/2}$, $m^* = 0.078 \text{ m}_0$ and its value is $5.7 \times 10^{17} \text{ cm}^{-3}$ for InP [17] at room temperature. The measured barrier heights of Au/P(VDC-MA)/n-InP Schottky devices are shown in Table-1.

In C-V technique, the carrier densities are less for annealed sample at 100 °C and for annealed sample at 150 °C when compared with as- deposited sample with values of Hall Measurements. This may be due to net electrically active doping concentration of donors' and acceptors. Because of the leakage current in Schottky devices, changes in capacitance measurements lead to subsequent error in doping concentration estimation. Dipole lowering effects due to charges image force lowering, leakage current and tunneling current reductions can be attributed to reduce SBH in J-V measurements. Calculated BH from capacitance-voltage measurements has influence on carrier trapping life time of the given InP semiconductor substrate. The calculated values of leakage current density, SBHs (J-V, Norde and C-V), series resistance (from dV/d (lnI) vs I) and ideality factor (n) of Au/P (VDC-MA)/n-InP Schottky device as a function of annealing temperatures are listed in Table-1.

4. CONCLUSIONS

Organic polyvinyl chloride polymers deposited directly on n-InP semiconductor substrate thereby capping layer of gold (Au) was deposited to obtain Schottky devices and studies as a function of annealing temperatures. From the experimental analysis, the high quality Schottky devices having BH of 0.85 eV using J-V, 0.96 eV using C-V, and ideality factor of 1.17, which are obtained when the sample is annealed at 100 °C for 1 min in nitrogen ambient. Similarly the BH is slightly lowered to 0.81 eV using J-V and 0.89 eV using C-V when annealed at 150 °C, respectively. Further using Norde function SBH is also calculated for Au/P(VDC-MA)/n-InP Schottky device. Nearly matching electronic parameters values such as ideality factor, barrier height and series resistance of the Schottky diode are obtained using J-V, using C-V and Norde method. This can be attributed due to modification by using a thin P(VDC-MA)organic layer in between Au/n-InP. The density of interface states have been calculated in forward bias using J-V as 2.018×10^{12} eV⁻¹cm⁻² for 100 °C and 1.842×10^{12} eV⁻¹cm⁻² for 150 °C annealed Au/P(VDC-MA)/n-InP Schottky devices. These results state that the interface states play a vital role in current flow mechanism in Schottky devices, and they should be kept as low as possible in order to reduce the surface recombination and tunneling.

ACKNOWLEDGEMENT

The first author thanks for sanction of Minor Research Project (MRP), No.F.MRP-3806/11/ (UGC-SERO) - pno.378 dated 8-9-2011, UGC-SERO, Hyderabad

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