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Efficient Implementation of Multi Stage SQRT Carry Select Adder

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Abstract: *To study the data dependence and to identify redundant logic operations, we are analysing logic operations involved in conventional carry select adder (CSLA) and binary to excess-1 converter (BEC)-based CSLA. A new logic formulation for CSLA has been proposed by eliminating all the redundant logic operations present in conventional CSLA. In the proposed scheme calculation of final-sum is scheduled after carry select (CS) operation we have eliminated all the redundant logic operations present in the conventional CSLA and proposed a new logic formulation for CSLA. Bit patterns of two anticipating carry words (corresponding to cin =0and1) and fixed in bits are used for logic optimization of CS and generation units, by using optimized logic units an efficient CSLA design is obtained The proposed CSLA design involves significantly less area and delay than the recently proposed BEC-based CSLA. The proposed CSLA design is best for square-root (SQRT) CSLA because of the small carry-output delay.*

Keywords: *conventional carry select adder, binary to excess-1 converter (BEC), proposed CSLA.*

1. Introduction

LOW-POWER, area-efficient, and high-performance VLSI systems are increasingly used in portable and mobile devices, multi standard wireless receivers, and biomedical instrumentation [1], [2]. An adder is the main component of an arithmetic unit. A complex digital signal processing (DSP) system involves several adders. An efficient adder design essentially improves the performance of a complex DSP system. A ripple carry adder (RCA) uses a simple design, but carry propagation delay (CPD) is the main concern in this adder. Carry look-ahead and carry select (CS) methods have been suggested to reduce the CPD of adders. A conventional carry select adder (CSLA) is an RCA–RCA configuration that generates a pair of sum words and output carry bits corresponding the anticipated input-carry (c in =0and1) and selects one out of each pair for final-sum and final-output-carry [3]. A conventional CSLA has less CPD than an RCA, but the design is not attractive since it uses a dual RCA. Few attempts have been made to avoid dual use of RCA in CSLA design. Kim and Kim [4] used one RCA and one add-one circuit instead of two RCAs, where the add-one circuit is implemented using a multiplexer (MUX). Heet al.[5] proposed a square-root (SQRT)-CSLA to implement large bit-width adders with less delay. In a SQRT CSLA, CSLAs with increasing size are connected in a cascading structure. The main objective of SQRT-CSLA design is to provide a parallel path for carry propagation that helps to reduce the overall adder delay. Ram Kumar and Kittur [6] suggested a binary to BEC-based CSLA. The BEC-based CSLA involves less logic resources than the conventional CSLA, but it has marginally higher delay. A CSLA based on common Boolean logic (CBL) is also proposed in [7] and [8]. The CBL-based CSLA of [7] involves significantly less logic resource than the conventional CSLA but it has longer CPD, which is almost equal to that of the RCA. To overcome this problem, a SQRT-CSLA based on CBL was proposed in [8]. However, the CBL-based SQRTCSLA design of [8] requires more logic resource and delay than the BEC-based SQRT-CSLA of [6]. We observe that logic optimization largely depends on availability of redundant operations in the formulation, whereas adder delay mainly depends on data dependence. In the existing designs, logic is optimized without giving any consideration to the data dependence. In this brief, we made an analysis on logic operations involved in conventional and BEC-based CSLAs to study the data dependence and to identify redundant logic operations. Based on this analysis, we have proposed a logic formulation for the CSLA. The main contribution in this brief is logic formulation based on data dependence and optimized carry generator (CG) and CS design based on the proposed logic formulation; we have derived an efficient logic design for CSLA. Due to optimized logic Units.

2. Existing CSLA

The structure of the 16-bit regular SQRT CSLA is shown in Fig. 4. It has 5 groups of different size RCA. Each group contains dual RCA and Mux. The linear carry select adder has two disadvantages there are high area usage and high time delay. SQRT CSLA can rectify these disadvantages of linear carry select adder. It is an improved one of linear CSLA. The time delay of the linear adder can decrease by having one more input into each set of adders than in the previous set. This is called a Square Root Carry Select Adder. Square Root carry select adder is constructed by equalizing the delay through two carry chains and the block-multiplexer signal from previous stage. The steps leading to the evaluations are given here. In the regular SQRT CSLA, the group2 has two sets of 2-bit RCA. The selection input of 3:2 Mux is c1. If the c1 = 0, the Mux select first RCA output otherwise it select second RCA output. The output of group2 is Sum [3:2] and carryout, c3. Then the area count of group2 is determined as follows:

Gate count = 57 (FA + HA + Mux)

FA = 39 (3 * 13)

HA = 6 (1 * 6)

Mux = 12 (3 * 4)

The structure of the 16-bit modified SQRT CSLA is shown in Fig. It has 5 groups of different size RCA and BEC. Each group contains one RCA, one BEC and MUX. In the modified SQRT CSLA, the group2 has one 2-bit RCA which has 1 FA and 1 HA for carry in = 0. Instead of another 2-bit RCA with carry in = 1 a 3-bit BEC is used which adds one to the output from 2-bit RCA. The selection input of 6:3 Mux is c3. If the c3 = 0, the Mux select RCA output otherwise it select BEC output. The output of group2 is Sum [3:2] and carryout, c3. Then the area count of group2 is determined as follows:

Gate count = 43 (FA + HA + Mux + BEC)

FA = 13 (1 * 13)

HA = 6 (1 * 6)

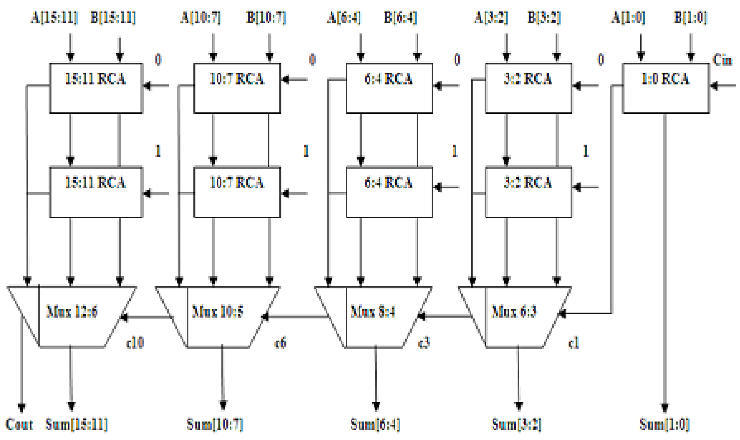
Mux = 12 (3 * 4)

NOT = 1

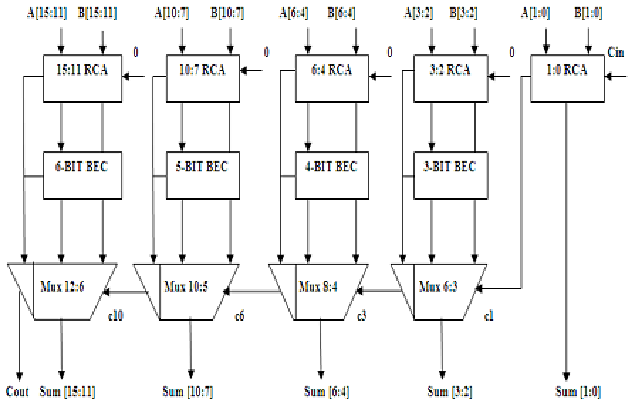
AND = 1

XOR = 10 (2 * 5)

BEC (3-BIT) = NOT + AND + XOR = 12



Regular 16-Bit SQRT CSLA

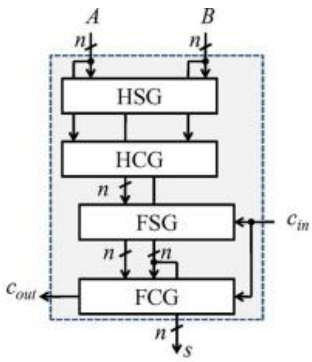


Modified 16-Bit SQRT CSLA

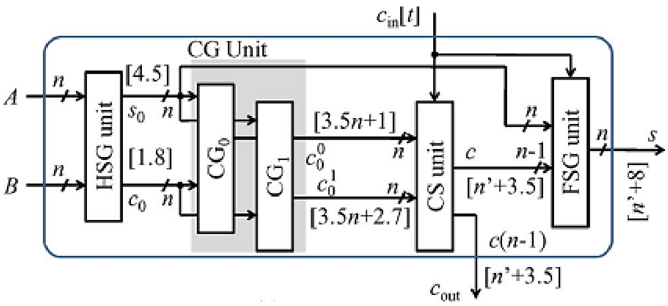
3. Proposed CSLA

The CSLA has two units: 1) the sum and carry generator unit (SCG) and 2) the sum and carry selection unit [9]. The SCG unit consumes most of the logic resources of CSLA and significantly contributes to the critical path. Different logic designs have been suggested for efficient implementation of the SCG unit. We made a study of the logic designs suggested for the SCG unit of conventional and BEC-based CSLAs of [6] by suitable logic expressions. The main objective of this study is to identify redundant logic operations and data dependence. Accordingly, we remove all redundant logic operations and sequence logic operations based on their data dependence.

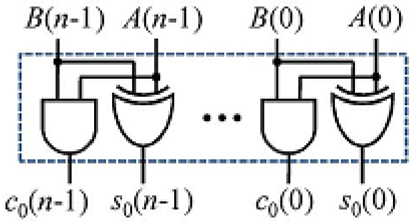
The proposed CSLA consists of one HSG unit, one FSG unit, one CG unit, and one CS unit. The CG unit is composed of two CGs (CG0and CG1) corresponding to input-carry ‘0’ and ‘1’. The HSG receives two n-bit operands (A and B) and generatehalf-sumwords0andhalf-carryword c0 of width n bits each. Both CG0and CG1receives0andc0 from the HSG unit and generate two n-bit full-carry wordsc01 andc11 corresponding to input-carry ‘0’ and ‘1’ respectively. The logic circuits of CG0and CG1are optimized to take advantage of the fixed input-carry bits. The optimized designs of CG0and CG1 .The multipath carry propagation feature of the CSLA are fully exploited in the SQRT-CSLA [5], which is composed of a chain of CSLAs. CSLAs of increasing size are used in the SQRT-CSLA to extract the maximum concurrence in the carry propagation path



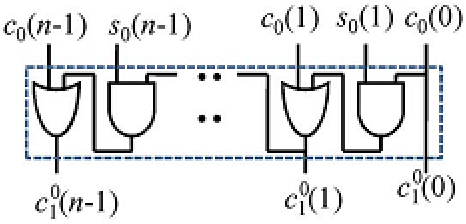
Proposed CS adder design



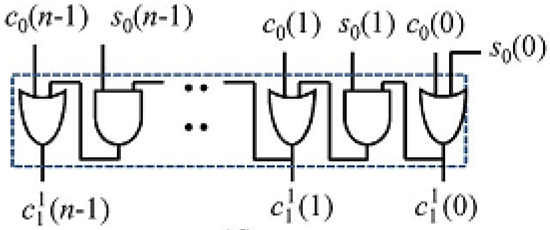
Gate-level design of the HSG



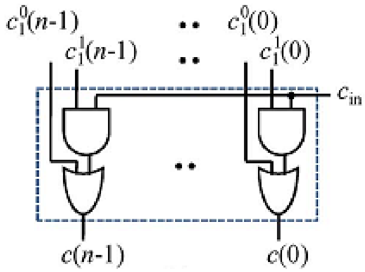
Gate-level optimized design of (CG0) for input-carry=0.



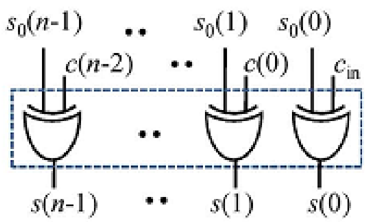
Gate-level optimized design of (CG1) for input-carry=1



Gate-level design of the CS unit

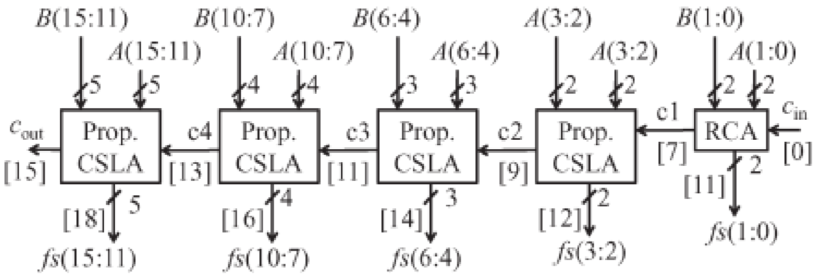


Gate-level design of the final-sum generation (FSG) unit



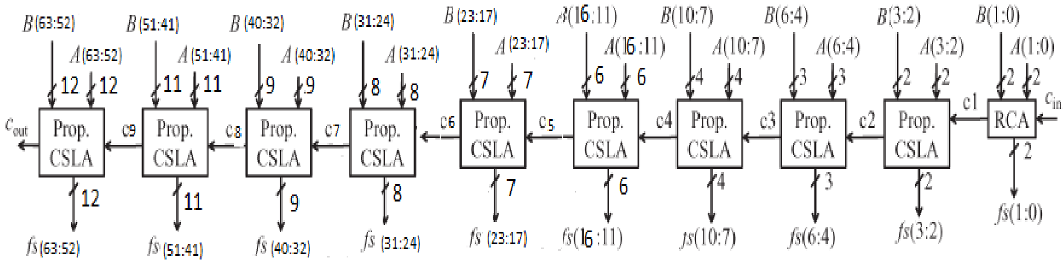
Proposed SQRT-CSLA for 16 bit

Using the SQRT-CSLA design, large-size adders are implemented with significantly less delay than a single-stage CSLA of same size. However, carry propagation delay between the CSLA stages of SQRT-CSLA is critical for the overall adder delay. Due to early generation of output-carry with multipath carry propagation feature, the proposed CSLA design is more favourable than the existing CSLA designs for area–delay efficient implementation of SQRT-CSLA. A 16-bit SQRT-CSLA design using the proposed CSLA is shown in Fig where the 2-bit RCA, 2-bit CSLA, 3-bit CSLA, 4-bit CSLA, and 5-bit CSLA are used. We have considered the cascaded configuration of (2-bit RCA and 2-, 3-, 4-, 6-, 7-and 8-bit CSLAs) and (2-bit RCA and 2-, 3-, 4-, 6-, 7-, 8-, 9-, 11-, and 12-bit CSLAs), respectively, for the 32-bit SQRTCSLA and the 64-bit SQRT-CSLA



Proposed SQRT-CSLA for 16 bit

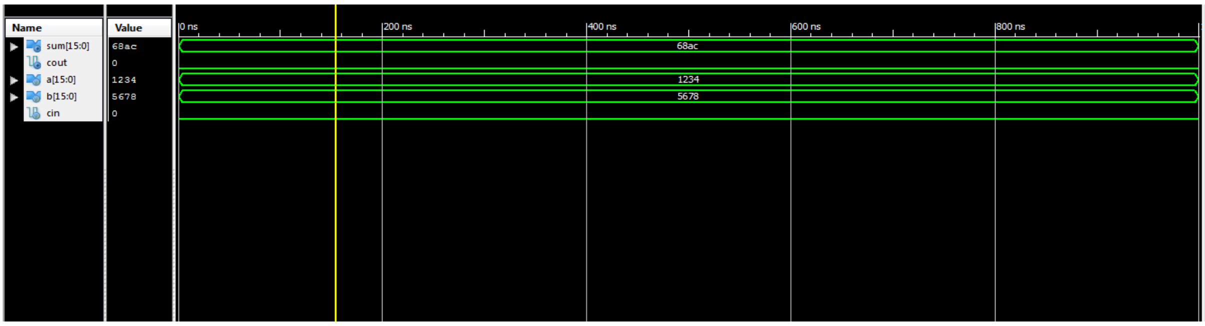
The logic operations of the RCA is shown in split form, where HSG, HCG, FSG, and FCG represent half-sum generation, half-carry generation, full-sum generation, and full-carry generation, respectively



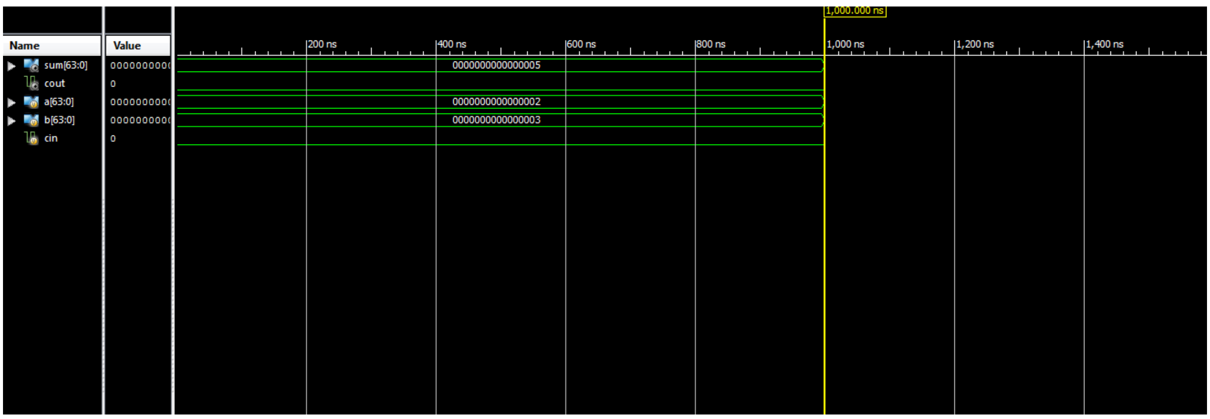
Proposed SQRT-CSLA for 64 bit

4. Results

Proposed SQRT-CSLA for 16 Bit Simulation



Proposed SQRT-CSLA for 64 Bit Simulation



5. Conclusion

We have analysed the logic operations involved in the conventional and BEC-based CSLAs to study the data dependence and to identify redundant logic operations. We have eliminated all the redundant logic operations of the conventional CSLA and proposed a new logic formulation for the CSLA. In the proposed scheme, the CS operation is scheduled before the calculation of final-sum, which is different from the conventional approach. Carry words corresponding to input-carry '0' and

'1'generated by the CSLA based on the proposed scheme follow a specific bit pattern, which is used for logic optimization of the CS unit. Fixed input bits of the CG unit are also used for logic optimization. Based on this, an optimized design for CS and CG units are obtained Using these optimized logic units, an efficient design is obtained for the CSLA. The proposed CSLA design involves significantly less area and delay than the recently proposed BEC-based CSLA. Due to the small carry output delay, the proposed CSLA design is a good candidate for the SQRT adder

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