International Journal of Research Studies in Science, Engineering and Technology
Volume 2, Issue 12, December 2015, PP 32-37
ISSN 2349-4751 (Print) & ISSN 2349-476X (Online)

Reduction of Leakage Power in Full Adder Circuit Using Power Gating Analysis

Ankammarao Gudi Seva

M.Tech, ECE Department, Malla Reddy Engineering College, Secunderabad, Telangana, India
ankammarao23@gmail.com

Abstract: *Adders area unit basic building block of Arithmetic VLSI circuits found in processors and microcontroller within Arithmetic and Logic units. Improvement of adder is so vital so as to extend the performance of those units wherever adders realize application. In this paper we show the reduction techniques of Leakage power suing Power gating Techniques. We apply the power gating techniques on the full adder and these circuits are designed and simulated using TSMC 018 technology using Tanner EDA tool.*

Keywords: *Full Adder, leakage power, Tanner EDA.*

1. INTRODUCTION

Adders are heart of machine circuits and plenty of complicated arithmetic circuits are supported the addition. The Brobdingnagian use of this operation in arithmetic functions attracts lots of researcher's attention to adder for mobile applications. In recent years, many variants of various logic designs are planned to implement 1-bit adder cells. These adder cells ordinarily aimed to scale back power consumption and increase speed. These studies have additionally investigated completely different approaches realizing adders mistreatment CMOS technology. For mobile applications, designers need to work at intervals a really tight discharge power specification so as to fulfill product battery life and package value objectives. The designer's concern for the extent of discharge current isn't associated with making certain correct circuit operation, however is expounded to reduce power dissipation. For transportable electronic devices this equates to increasing battery life. for instance, mobile phones ought to be supercharged for extended periods (known as standby mode, throughout that the phone is in a position to receive Associate in Nursing incoming call), however are totally active for a lot of shorter periods (known as speak or active mode, whereas creating a call) When Associate in Nursing device like a mobile is in standby mode, sure parts of the circuitry at intervals the device, that ar active once the phone is in speak mode, ar stop working. These circuits, however, still have discharge currents running through them, even if they need been de-activated. Albe it the discharge current is way smaller than the conventional operative current of the circuit. The discharge current depletes the battery charge over the comparatively long standby time, whereas the operative current throughout speak time solely depletes the battery charge over the comparatively short speak time. As a result, the discharge current includes a disproportionate result on total battery life. this can be why building low discharge adder cells for mobile applications ar of nice interest. To summarize, some performance criteria ar thought-about within the style and analysis of adder cells, like discharge power, active power, ground bounce noise, area, noise margin and lustiness with relation to voltage and semiconductor device scaling additionally as varied method and compatibility with encompassing circuitries. Shortening the gate length of a semiconductor device will increase its power consumption because of the exaggerated discharge current between the transistors supply and drain once no signal voltage is applied at the gate. additionally to the sub threshold discharge current, gate tunneling current additionally will increase because of the scaling of gate chemical compound thickness. every new technology generations results nearly a 30xincrease in gate discharge.

The power reduction should be achieved while not trading-off performance that makes it more durable to scale back run throughout traditional (runtime) operation. On the opposite hand, there square measure many techniques to scale back run power. Power gating is one such accepted technique wherever a sleep electronic transistor is additional between actual ground rail AND gate ground (called virtual ground). This device is turned off within the sleep mode to cut-off the run path. It's been shown that this system provides a considerable reduction in run at a smallest impact on performance and additional peak of ground bounce noise is feasible with planned novel technique with improved staggered part damping technique.

This paper organized as chapter-I deal about the introduction, chapter-II describes the estimator methodology, chapter-III the proposed method followed by the results and discussion, conclusion and references.

1-Bit Full Adder:

A one-bit full adder could be a device with 3 single bit binary inputs (A, B, Cin) and 2 single bit binary outputs (Sum, C-out). Having each carry in and perform capabilities, the total adder is extremely ascendible and located in several cascaded circuit implementations.

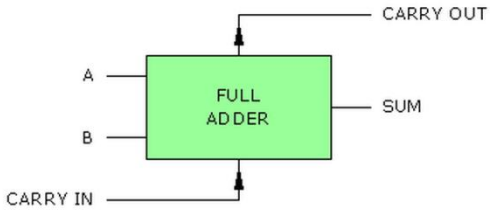

Fig1. *Symbol of 1-Bit Full Adder*

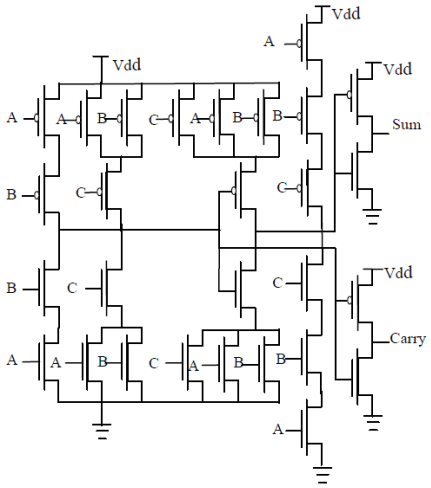

Fig2. *28T Conventional Full adder*

The above shown standard full adder is combination of PMOS pull up junction transistor and NMOS pull down transistor. It's acknowledge for its hardiness and measurability at low offer voltages. However its power consumption and semiconductor count ar comparatively high for low power arithmetic circuits. During this full adder, reciprocality between signals generation (SUM signal depends on the generation of COUT signal) causes the matter of delay imbalance.

Power gating technique is employed to cut back the run power, wherever a sleep semiconductor device is connected between actual ground rail AND circuit ground. Ground bounce noise is being calculable once the circuits ar connected with a sleep semiconductor device. Further, the height of ground bounce noise is achieved with a planned novel technique. changed sizings ar shown in following figures severally.

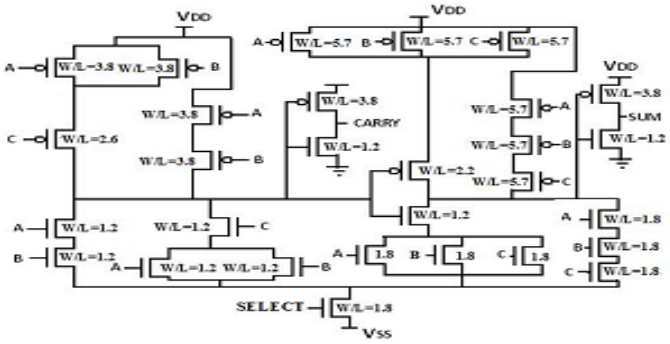

Fig3. *Full adder (Design1) circuit with sleep transistor*

Each block has been treated as identical electrical converter. Identical electrical converter magnitude relation is maintained on every block. These size can scale back the standby leak current greatly as a result of subthreshold current is directly propotional to the Width/Length magnitude relation of junction transistor. On the opposite hand, these scale backd sizes can reduce the world occupied by the circuit. This may scale back the chip space and clearly there'll be a discount within the price. changed adder circuit i.e Design2 shown figure, the W/L magnitude relation of PMOS is one.5 times that of W/L magnitude relation of NMOS and every block has been treated as identical electrical converter. The goal of this style is to cut back the standby leak power. additional compared to the bottom case and Design1 and ground bounce noise made once a circuit is connected to sleep junction transistor. However, there'll be a small variation on the noise margin levels and is nearly capable the bottom case.

2. ESTIMATOR METHODOLOGY

2.1. Existing Designs of Power Gating Circuits

- Sleepy Stack Approach
- Leakage Feedback
- Leakage Feedback with stack
- Dual Stack
- Stacked Sleep

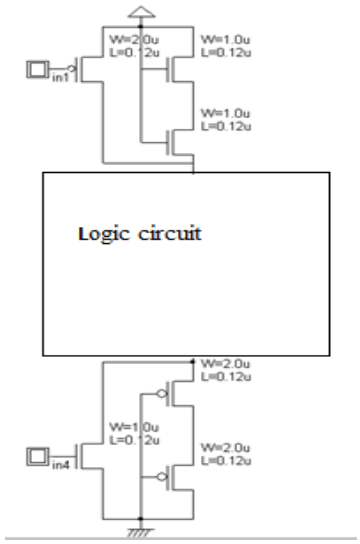

Fig4. *Dual Stack Approach*

A variation of the sleep approach, the zigzag approach, reduces wake- up overhead caused by sleep transistors by placement of alternating sleep transistors presumptuous a specific pre-selected input vector [6]. Another technique for escape power reduction is that the stack approach, that forces astack result by breaking down associate degree existing junction transistor into 2 [*fr1] size transistors [7]. The divided transistors increase delay considerably and will limit the quality of the approach. The sleepyheaded stack approach (Fig. 2) combines the sleep and stack approaches [2, 3]. The sleepyheaded stack technique divides existing transistors into 2 [*fr1] size transistors just like the stack approach. Then sleep transistors square measure side in parallel to at least one of the divided transistors. throughout sleep mode, sleep transistors square measure turned off and stacked transistors suppress escape current whereas saving state. every sleep junction transistor, placed in parallel to the one in all the stacked transistors, reduces resistance of the trail, thus delay is small throughout active mode. However, space penalty could be a vital matter for this approach since each junction transistor is replaced by 3 transistors and since further wires square measure side for S and S', that square measure sleep signals. Another technique known as twin sleep approach [8] (Fig. 3) uses the advantage of victimisation {the 2|the 2} further pull- up and two further pull-down transistors in sleep mode either in OFF state or in ON state. Since the twin sleep portion are often created common to all or any logic electronic equipment, less range of transistors is required to use a definite logic circuit.

3. PROPOSED METHOD

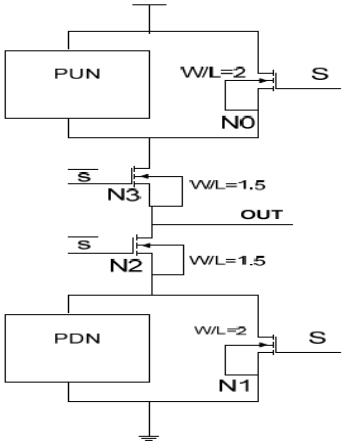

Fig5. *Proposed Design*

The projected technique consists of 2 NMOS semiconductor devices N2 and N3 that acts sort of a staking theme and 2 NMOS transistors as N0 and N1 transistors as helper transistor to extend the output voltage of the circuit

4. SIMULATION RESULTS

These circuits are designed and simulated using S-Edit Tanner tools and Done T-Spice simulation

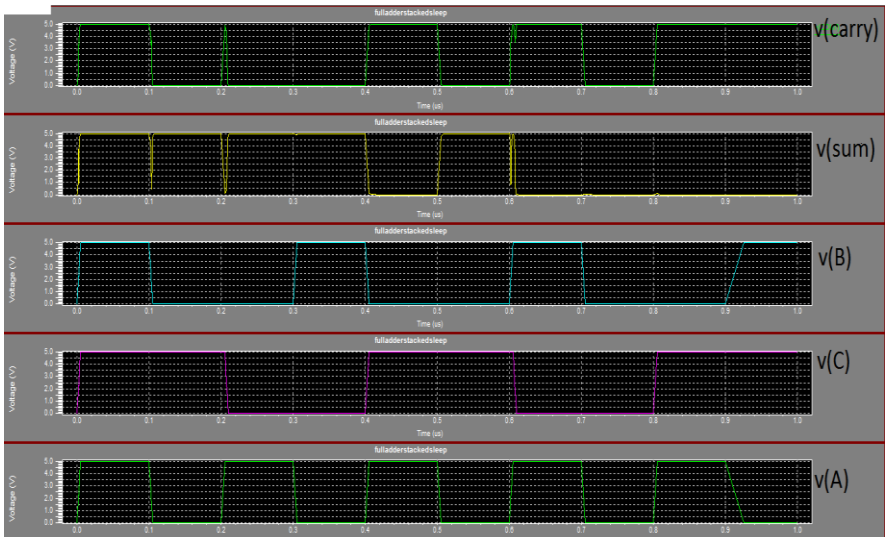

Fig7. *Wave form of Full Adder*

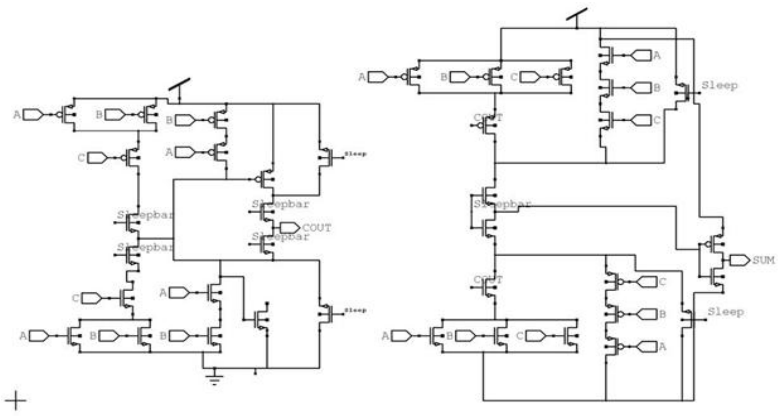

Fig8. *S-Edit Design of Proposed Full Adder*

Tabulation:

This Full adder Circuit was designed using above power gating techniques using S-Edit and Simulation was carried out using T-Spice

Table1. *Output result*

Circuit	Power Dissipation
Full Adder	2.357744e-004 watts
Full Adder Sleep Keeper	8.359430e-005 watts
Full Adder Leakage Feedback	8.300160e-007 watts
Full Adder with Stacked Sleep	1.000681e-006 watts
Full Adder Dual Stack	6.996312e-008 watts
Proposed Full Adder	6.549149e-010 watts

5. CONCLUSION

In nm scale CMOS technology, subthreshold run power consumption could be a nice challenge. Though previous approaches square measure effective in some ways in which, no good resolution for reducing run power consumption is nevertheless notable. Therefore, designers opt for techniques primarily based upon technology and style criteria. During this paper, we provide novel circuit as a brand new remedy for designers in terms of static power and dynamic powers. Not like the sleep semiconductor technique, the twin stack technique retains the initial state. The twin stack approach shows the smallest amount speed power product among all ways. Therefore, the twin stack technique provides new ways in which to designers World Health Organization needs ultra-low run power consumption with a lot of less power.

REFERENCES

[1] M. Powell, S.-H. Yang, B. Falsafi, K. Roy and T. N. Vijaykumar, "Gated-Vdd: A Circuit Technique to Reduce Leakage in Deep submicron Cache Memories," Proc. of International Symposium onLow Power Electronics and Design, pp. 90-95, July 2000.

[2] J.C. Park, V. J. Mooney III and P. Pfeiffenberger, "Sleepy Stack Reduction of Leakage Power," Proc. of the International Workshop onPower and Timing Modeling, Optimization and Simulation, pp. 148-158, September 2004.

[3] J. Park, "Sleepy Stack: a New Approach to Low Power VLSI and Memory," Ph.D. Dissertation, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2005. [Online].Available http://etd.gatech.edu/theses.

[4] S. Mutoh, T. Douseki,. Y. Matsuya, T. Aoki, S. Shigematsu and J. Yamada, "1-V Power Supply High-speed Digital Circuit Technology with Multithreshold-Voltage CMOS," IEEE Journal of Solis-StateCircuits, vol. 30, no. 8, pp. 847–854, August 1995.

[5] N. Kim, T. Austin, D. Baauw, T. Mudge, K. Flautner, J. Hu, M. Irwin, M. Kandemir and V. Narayanan, "Leakage Current: Moore's Law Meets Static Power," IEEE Computer, vol. 36, pp. 68–75, December 2003.

[6] S. Kim, S. V. Kosonocky, D. R. Knebel, K. Stawiasz, D. Heidel, and M. Immediato, "Minimizing inductive noise in system-on-a-chip with multiple power gating structures," in Proceedings of European Solid-State Circuits: pp. 16-18, 2003.

[7] A Kabbani and A J. AI-Khalili "Estimation Ground Bounce Noise Effect on CMOS Circuits," IEEE Transactions on Components and Packaging Technology, vol. 22, pp. 316-325, June 1999

[8] N. Karmakar, M. Z. Sadi, M. K. Alam and M. S. Islam, "A novel dual sleep approach to low leakage and area efficient VLSI design" Proc.2009 IEEE Regional Symposium on Micro and Nano Electronics (RSM2009), Kota Bharu, Malaysia, August 10-12, 2009, pp. 409-414.

[9] Avant!Corporation,http://www.avanticorp.com

[10] http://www.eas.asu.edu/~ptm/

[11] J. Shin and T. Kim, "Technique for transition energy-aware dynamic voltage assignment," IEEE Trans. Integr. Circuits Syst. II, Exp. Briefs,vol. 53, no. 9, pp. 956–960, Sep. 2006.

[12] W. Cheol and T. Kim, "Optimal voltage allocation techniques fordynamically variable voltage processors," ACM Trans. EmbeddedComput. Syst., vol. 4, no. 1, pp. 211–230, Feb. 2005.

[13] T. Ishihara and H. Yasuura, "Voltage scheduling problem for dynamically variable voltage processors," in Proc. IEEE/ACM Int. Symp. LowPower Electron. Des., 1998, pp. 197–202.

[14] F. Fallah and M. Pedram, "Standby and active leakage current control and minimization CMOS VLSI circuits," IEICE Trans. Electron., vol.E88-C, no. 4, pp. 509–519, 2005.

[15] J. Friedrich, B. McCredie, N. James, B. Huott, B. Curran, E. Fluhr, G.Mittal, E. Chan, Y. Chan, D. Plass, S. Chu, H. Le, L. Clark, J. Ripley, S.Taylor, J. Dilullo, and M. Lanzerotti, "Design of thePower6 microprocessor,"inProc. IEEE/ACM Int. Solid-State Circuits Conf., Feb. 2007,pp. 96–97.

[16] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamada,"1-V power supply high-speed digital circuit technology with multi-threshold voltage CMOS," IEEE J. Solid-State Circuits, vol. 30, no. 8, pp. 847–854, Aug. 1995.

[17] J. Kao, A. Chandrakasan, and D. Antoniadis, "Transistor sizing issues and tool for multi-threshold CMOS technology," in Proc. IEEE/ACMDes. Autom. Conf., 1997, pp. 409–414.