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FIR Filter for Wireless Sensor Networks with Appraise Characteristics

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Abstract: *There are different deep progressed researches on the FIR filters for the improvement of the panoramas of VLSI. As the part of the problem solving different solutions, cerebrations will be projected like parallel operated, poly decomposed. For some application slow and less power filter artifact and improved multiplication dodge will be introduces such as booth algorithm, Vedic and MCM bases multiplication and more. But these are not well suited for the Wireless sensor network, because naturally this consists of the slender and more, we cannot provide large power. From these appraise, we notice that wireless sensor networks goes one foot back, hence our proposal we treated a new method of FIR construction by using the MCM base shift-add algorithm with reduced latency and flop count, with this above retreat can be subdue.*

1. INTRODUCTION

Finite Impulse Response (FIR) digital filters are extensively used in digital signal processing systems, ranging from video and image processing to wireless communication.

Fast parallel filter is designed with significant number of approaches. Short convolution algorithms are applied to attain parallel filters with fewer computations. Poly phase decomposition and fast FIR algorithm (FFA) has been adapted to design parallel FIR filters.FFA algorithm is more reliable while computing the large block sizes.

Parallel FIR filters can be implemented by a set of fast block filtering algorithms in association with linear convolution algorithms. Increasing the convolution length cause to increase the number of additions results its complexity in computations.The proposed shift-add method is to implement N-tap FIR filters for FPGA's to enhance the filters processing speed and condense the computation time.

In this method each "1" in the binary representation of the coefficients, agreeing to its bit location, input data can be shifted and add with the previous shifted value. The shifts-add method required one adder in addition to a shifter and minimizes the multiplier number to zero and its area. However no more multipliers are implied in our FIR filter structures.

The proposed FIR filter structure is very efficient in reducing hardware cost and energy consumption, especially when the length of the FIR filter is large. FPGAs are being increasingly used for a variety of computationally intensive applications, mainly in the realm of Digital Signal Processing (DSP) and communications. Due to rapid increases in the technology, current generation of FPGAs contain a very high number of Configurable Logic Blocks (CLBs), and are becoming more feasible for implementing a wide range of applications

2. FILTER ALGORITHM

There are basic two FIR structures, direct form and transposed form, shown in Fig.1 for a linear-phase even-order FIR Filter. In the direct form in Fig. 1(a), the multiple constant multiplication (MCM)/

accumulation (MCMA) module performs the concurrent multiplications of individual delayed signals and respective Filter coefficients, followed by accumulation of all the products.

Base-forming of hardware overhead conditions the FIR structures are classified into basic two types based on the utility of costly multipliers, they are multiplier-less based and memory based.

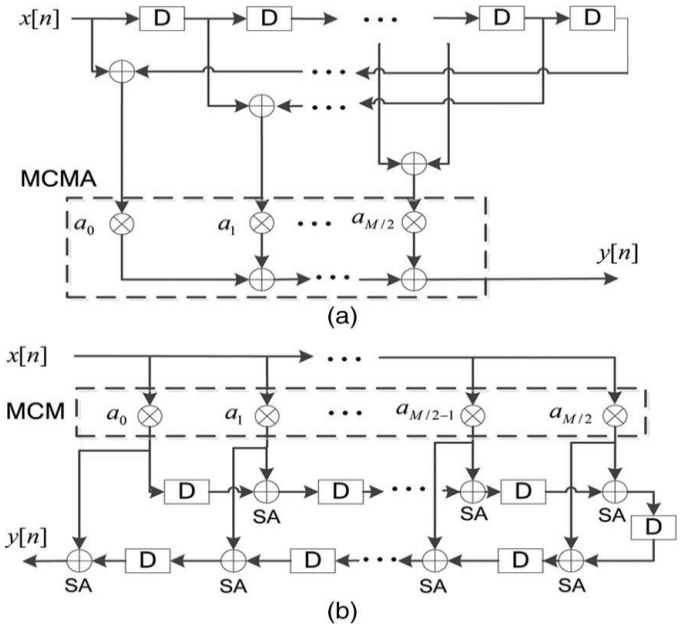

Fig1. *Structures of linear-phase even-order FIR Filters: (a) Direct form and(b) transposed form.*

Basic constant multiplications carry out by the structure adders (SAs) and delay elements. In this the Filter coefficients are fixed hence called as the multiple constant multiplications.

For better design strategies of the multiplier-less based filter resent proposals introduces MCM with shift-and add operations and shares the common sub-operations using common sub-expression elimination (CSE) and canonical signed digit (CSD) recoding to minimize the added cost of MCM [8].

For design of the reserve multiplier less filters, we take such considerations and stepwise design stages are listed below. By this the suitable design can be designed by the advanced and the less utilization of the adder elements in the proposed design. For the design of MCM basically filter coefficients are fixed, as the first step we need to calculate the appropriate filter coefficient for regarded to the response which should acquire the suited order.

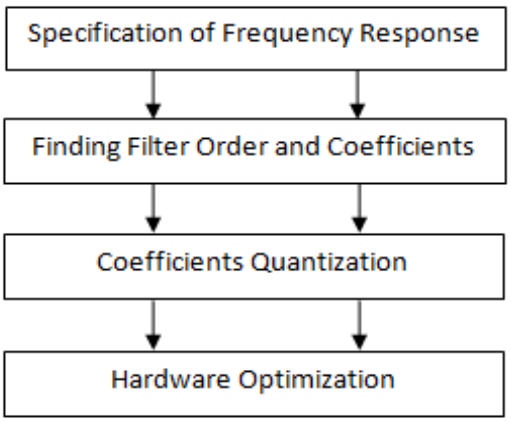

Fig2. *Stages in digital FIR Filter design and implementation.*

After coefficient determination, response quantization factor should be analyzed then the hardware optimized conditions can be verified and suited parallel utilized pipelined architecture can be designed. For the design, in these also two considerations can be recommended based on the area and the power, those are bit-serial, bit-parallel, parallel pipelined, serial pipelined and inter utilized operational architecture which will undergone by the function based architecture construction .

3. SERIAL COEFFICIENT CALCULATION

In our proposed design we consider the 8- tap low-pass FIR filter and the coefficients can be calculated by using MATLAB using Remez Exchanging algorithm the maximum absolute difference (MAD) algorithm introduced in [1] is used for coefficients quantization.

Then the coefficients can be optimized and converted into the binary fixed point representation format. In order to make the coefficients into the fixed point representation, can be calculated with area and power optimized algorithms for the efficient design to the requirements suited for the commanded application.

Assuming that the coefficients of an 8-tap FIR filter are0.3759, 0.3086, -0.1255, 0.06439, 0.2187, 0.0168, -0.00415and 0.01758. And then their binary representations can beexpressed as,

$$h(0) = 0.3759 = 2^{-1}+(-2^{-3})+2^{-10}$$
$$h(1) = 0.3086 = 2^{-2}+2^{-4}+(-2^{-8})$$
$$h(2) = -0.1255 = -2^{-3}+(-2^{-11})$$
$$h(3) = 0.6439 * 10^{-1} = 2^{-4}+2^{-9}$$
$$h(4) = 0.2187 = 2^{-2}+(-2^{-5})$$
$$h(5) = 0.0168 = 2^{-6}+2^{-10}+2^{-12}$$
$$h(6) = -0.415 * 10^{-2} = -2^{-8}+(-2^{-12})$$
$$h(7) = 0.1758 * 10^{-1} = 2^{-6}+2^{-9}$$

$$y(n) = (2^{-1}-2^{-3}+2^{-10})*x(n)+(2^{-2}+2^{-4}-2^{-8})*x(n-1)+(-2^{-3}-2^{-11})$$
$$*x(n-2)+(2^{-4}+2^{-9})*x(n-3)+(2^{-2}-2^{-5})*x(n-4)+(2^{-6}+2^{-10}$$
$$+2^{-12})*x(n-5)+(-2^{-8}-2^{-12})*x(n-6)+(2^{-6}+2^{-9})*x(n-7)$$

Obviously, all the inputs should be multiplied by a sequence of numbers that are specific powers of 2, what's more, some inputs should be multiplied by the same number, for instance, both x(n) and x(n-2) have to multiply by -2, so we can get all the inputs that have to multiply by the same number together. In this way, we can get, which is shown as follows.

$$y(n) = 2^{-1}*x(n)+2^{-2}*(x(n-1)+x(n-4))+x^{-3}(-x(n)-x(n-2))$$
$$+2^{-4}*(x(n-1)+x(n-3))-2^{-5}*x(n-4)+2^{-6}*(x(n-5)+$$
$$x(n-7))-2^{-8}*x(n-1)+2^{-9}*(x(n-3)+x(n-7))+2^{-10}*$$
$$(x(n)+x(n-5))-2^{-11}*x(n-2)+2^{-12}*(x(n-5)-x(n-6))$$

From the above the design can be carried out by the sub splitting the operations in such a way those operations can be done by only with the one shifting and the respected addition.

The above conserved equation be re-modified is as followed

$$y(n) = 2^{-1} * (\ldots (2^{-1} * (2^{-1} * U_1 + U_2) + U_3) + \ldots + U_{12})$$

where U1 = x(n-5)-x (n-6); U2 = -x (n-2);
U3 = x (n) +x (n-5); U4 = x (n-3) +x (n-7);
U5 = -x (n-1); U6 = 0;
U7 = x (n-5) +x (n-7); U8 = -x (n-4);
U9 = x (n-1) +x (n-3); U10 = - x (n)+(-x (n-2))
U11 = x (n-1) +x (n-4); U12 = x (n);

In order to design the specified filter and with nominated tap and the bit length there by the architecture may under gone the specified changes were made with respect to that. When you want to design the filter coefficients can be calculated and the required conditions along with the repeated conditional methods that will associate to the design of the specified equation.

4. PROPOSED METHOD

In this method when start asserted the design will take 8-inputs each of 8-bits consecutively from the counter. The counter logic generates the read address for the data Ram until the count reaches the count '8'.

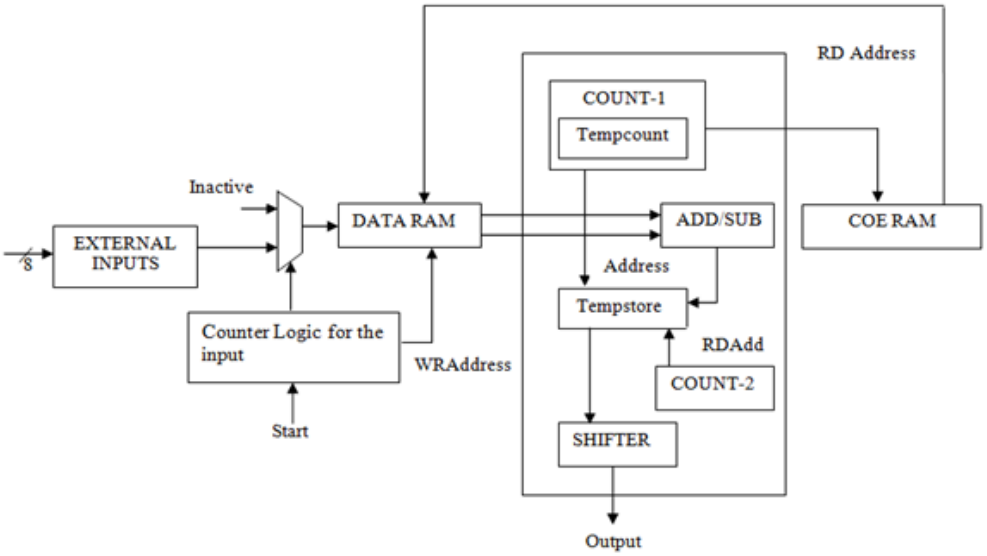

Fig3. *Proposed filter architecture*

After storing all inputs in the Data Ram the count-1 will start the count that will be the address for the coefficient. Then based on the output of the coefficient RAM the data can be read from the ROM. Here the important consideration it from the coefficient ROM, it generates the two data address, in order to read the two data from the data Ram, the temp_count will be used. Then those will be added or subtracted based on the sign determined in the coefficient ROM and stored in the temp_store based on the count-1 as address. After that the count-2 starts counting that will be read address for the temp_store. The data read from the temp_ store can be shifted with respect to the count-2 at the end, produces the output.

5. RESULTS AND DISCUSSION

We have taken input as 10101010. Initial reset has been given as 1, hence all the memories, signals and flip flops are initialized to 0 and coefficients are stored in the memory2.

After one clock cycle reset is given as 1, and then inputs are loaded into data RAM. For each clock cycle inputs are read from data RAM and coefficients are read coefficient RAM.

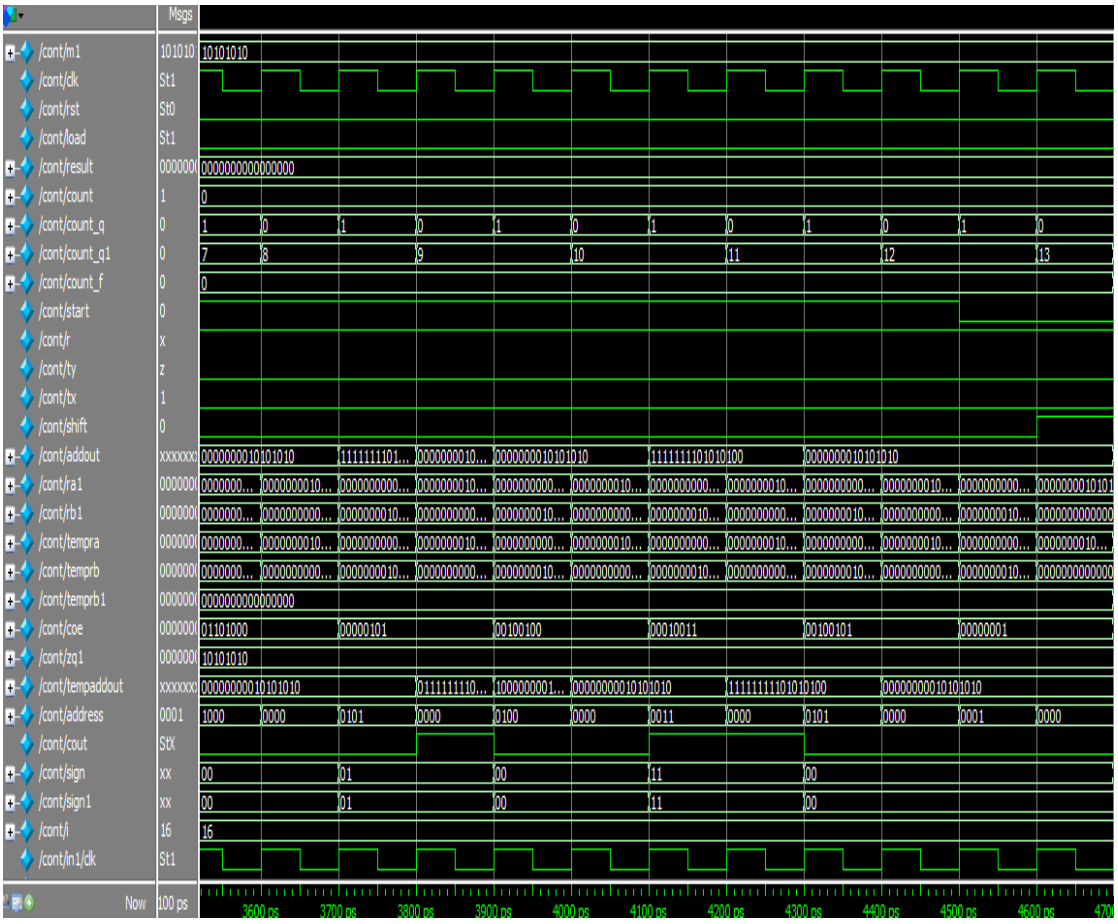

Fig4. *Intermediate result*

Based on coefficient RAM output operation will be performed and stored in the memory. Shifted operation will be performed from the above memory to obtain the final output.

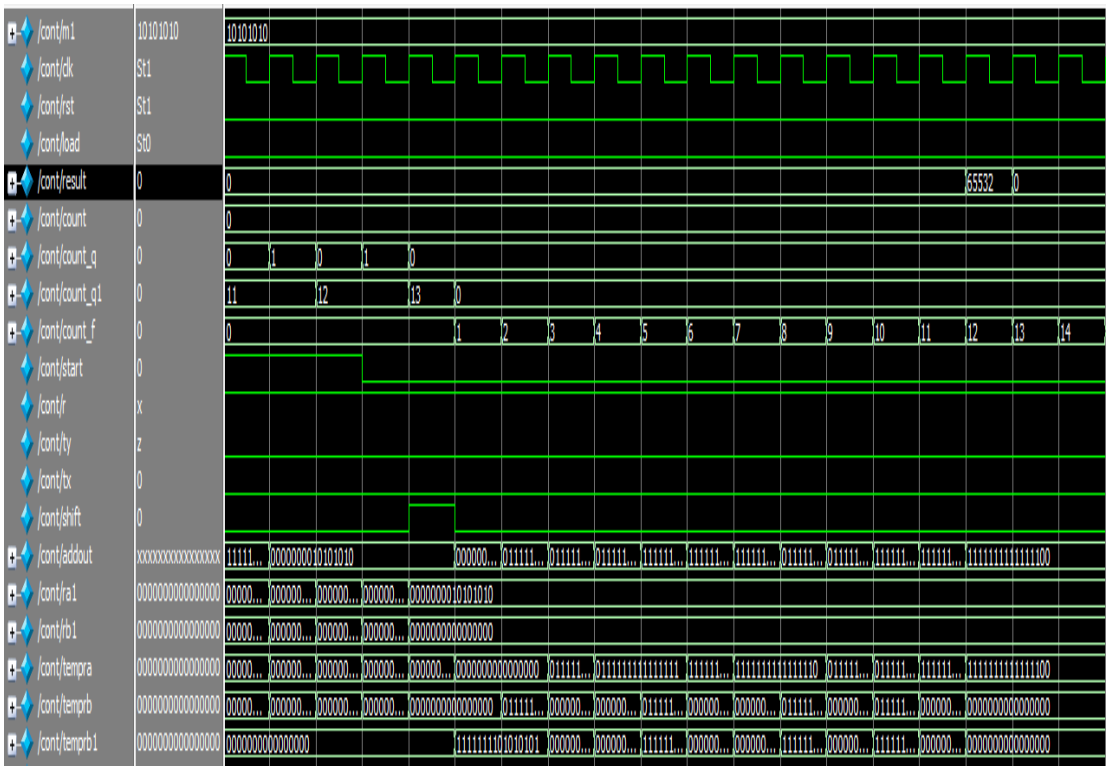

Fig5. *Final result*

Synthesis comparisons

The synthesis comparisons of the existing and the proposed methods with 8 tap and 16 tap multipliers are given in the following tables.

Design	Tap	slices
Previous [11]	8 tap	380
Proposed	8 tap	364
Design	Tap	slices
Fir filter with multiplier	16 tap	656
Proposed	16 tap	1480

6. CONCLUSION

FIR filter for wireless sensor networks and also low power application based on the proposed method were designed. In our method no longer multipliers were used and pipelined operation can be adopted for the improvement of the speed of operation. In our design the temp_count concept used by this two data can be read from the data RAM there by one clock latency can be reduced for the all read operation of the data RAM. As from the previous no multiplier and only one adder along with shifter are used there by no vary for the foot print increase. But here further more latency can be reduced with improved performance.

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